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| APPLICATION NO.  | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO.             | CONFIRMATION NO.            |
|--|-------------|----------------------|---------------------------------|-----------------------------|
| 10/710,490   | 07/15/2004  | Ching-Yen Wu         | VIAP0116USA                     | 4489                        |
| 27765 7590 06/28/2007<br>NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION<br>P.O. BOX 506<br>MERRIFIELD, VA 22116 |             |                      | EXAMINER<br>SINGH, HIRDEPAL     |                             |
|  |             |                      | ART UNIT<br>2611                | PAPER NUMBER                |
|  |             |                      | NOTIFICATION DATE<br>06/28/2007 | DELIVERY MODE<br>ELECTRONIC |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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|                              |                                      |                                      |  |
|------------------------------|--------------------------------------|--------------------------------------|--|
| <b>Office Action Summary</b> | <b>Application No.</b><br>10/710,490 | <b>Applicant(s)</b><br>WU, CHING-YEN |  |
|                              | <b>Examiner</b><br>Hirdepal Singh    | <b>Art Unit</b><br>2611              |  |

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 15 July 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-10 is/are pending in the application.  
     4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 July 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
     a) ☒ All    b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

This action is in response to the original filing date of July 15, 2004. Claims 1-10 are pending in the application, and have been considered below.

### ***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 2, 4, and 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Hendrickson (US 2002/0090045).

Claim 1: Applicant's Admitted Prior Art (AAPA) discloses a clock and data recovery circuit recovering a clock signal embedded in the incoming data stream (Description of Prior Art) comprising;

- a. a phase shifter i.e. a circuit for generating discrete clocks at different phases equally spaced in time (figure 1; page 2, paragraph 0006);
- b. a data sampler generating a signal i.e. select signal according to input data stream and discrete clocks (figure 1; page 3, paragraph 0006);

c. AAPA discloses a data sampler, and phase selector, but doesn't explicitly disclose that a primary phase selector is receiving inputs from a phase shifter, and a data sampler and outputting discrete clocks and an interpolated clock to multiplexer. However, Hendrickson discloses a similar clock and data recovery circuit where a selector is used to select a signal based on the phase difference signal and plurality of clock signals (paragraphs 0015-0016; figures 1-3), and further discloses that the multiple discrete clocks are interpolated to generate a clock signal with finer steps or with smaller delay or phase differences (paragraph 0025). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the phase selector and interpolator in AAPA in order to avoid the false locking of the recovered clock and also to save power and chip area by using less complex circuitry;

d. AAPA further discloses, a multiplexer for selecting one of the discrete clocks as a recovered clock signal (figure 1; page 3, paragraph 0006), but doesn't explicitly disclose that the multiplexer could select one of the discrete clocks or the interpolated clock. However, Hendrickson discloses a similar clock and data recovery circuit where a selector is used to select a signal based on the phase difference signal and plurality of clock signals (paragraphs 0015-0016; figures 1-3), and further discloses that the multiple discrete clocks are interpolated to generate a clock signal with finer steps or with smaller delay, and a multiplexer selects a signal from the delayed signals i.e. it could a discrete signal or a interpolated signal (paragraphs 0025-0029). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention

was made to use the multiplexer in AAPA in order to select a required clock from the discrete clocks or the interpolated clock;

e. AAPA further discloses, a phase detector receiving the recovered clock from multiplexer and outputting a signal i.e. an advanced signal if the recovery clock leads or lags the input data stream (figure 1; page 3, paragraph 0006);

f. AAPA further discloses, a phase selector for receiving advanced calibration signal i.e. signal from phase detector and transmitting the phase select signal to the multiplexer (figure 1; paragraph 0006), but doesn't explicitly disclose transmitting a signal to primary phase selector for adjusting the discrete clocks and corresponding interpolated clock. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to adjust the primary phase selector of AAPA, and Hendrickson system (as described above in c) if the recovered clock leads or lags the in coming data stream i.e. if the phase difference is such that the in coming data is not falling in the consecutive phase steps i.e. the recovered signal phase is not falling between the consecutive clock phases. One would have been motivated to adjust the phase selector in order to switch it to the next or previous phase step depending on if the recovered signal is leading or lagging the input.

Claim 2: AAPA, and Hendrickson disclose a clock and data recovery circuit as in claim 1 above, and Hendrickson further discloses an analog phase locked loop used in the data recovery circuit, and the PLL uses analog components (paragraphs 0004-0005).

Therefore, it would have been obvious to one having ordinary skill in the art at the time

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the invention was made to use the analog PLL in AAPA in order to save chip area, power, and to be able to operate at high frequencies.

Claim 4: AAPA, and Hendrickson disclose a clock and data recovery circuit as in claim 1 above, and AAPA further discloses the data sampler using a number of edge triggered flip-flops where the incoming data stream is input to clock inputs and the discrete clocks are input to data input ends of the flip-flops (figure 3; pages 3-4, paragraph 0007).

Claim 5: AAPA, and Hendrickson disclose a clock and data recovery circuit as in claim 4 above, and AAPA further discloses using a number of edge triggered flip-flops are D flip-flops (figure 3; pages 3-4, paragraph 0007).

Claim 6: AAPA, and Hendrickson disclose a clock and data recovery circuit as in claim 1 above, and AAPA further discloses using recovery clocks to trigger the input data to form recovery data (page 5, paragraph 0008).

Claim 7: AAPA, and Hendrickson disclose a clock and data recovery circuit as in claim 1 above, and AAPA further discloses a counter connected between the data sampler and phase detector for stability of input data and inputting data to data sampler (figure 1; pages 2-3, paragraph 0006).

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3. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Hendrickson (US 2002/0090045) further in view of Lee et al. (US 2002/0085656).

Claim 3: AAPA, and Hendrickson disclose a clock and data recovery circuit as in claim 1 above, but neither explicitly discloses that the phase shifter is a delay-locked loop (DLL). However, Lee discloses a similar clock and data recovery system in the background of invention, where a delay-locked loop (DLL) is used in the phase shifter (paragraph 0008). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a delay-locked loop (DLL) in AAPA system. One would have been motivated to use a delay-locked loop (DLL) in the phase shifter to generate plurality of phase shifted clocks in order to get the error to go to zero while keeping the control signal, and the delays, where they need to be for phase lock.

4. Claims 8, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Hendrickson (US 2002/0090045) further in view of Chen (US 5,850,422).

Claim 8: AAPA, and Hendrickson disclose a clock and data recovery circuit as in claim 1 above, but neither explicitly disclose that the calibration signal is output as plus 1 or minus 1. However, Chen discloses a similar clock and data recovery apparatus, and further discloses that the function of lead/lag phase detector as, when recovery clock



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leads or lags the incoming data stream the lead/lag phase detector transmits lead or lag signal (active high or low) accordingly, to adjust the phase of recovery clock (figures 6a, 6b; column 6, lines 37-65), but doesn't explicitly disclose that when recovery clock lags the input clock the output of phase detector goes to plus one. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to implement the system to transmit a plus 1 or minus 1 as a calibration signal depending on the phase difference between recovery clock and input data (leading or lagging) in AAPA. One would have been motivated to use a plus 1 or minus 1 as calibration signal in order to control the phase of recovery clock.

Claim 9: AAPA, Hendrickson, and Chen disclose a clock and data recovery circuit as in claim 8 above, and Chen further discloses that the signal going into the multiplexer from shift register loop filter is modified according to advanced calibration signal i.e. the signal from phase detector (figure 1; column 2, lines 40-52), but doesn't explicitly disclose that when both discrete clocks and the interpolated clock according to phase select signal lead or lag input data, the advanced phase selector outputs primary calibration signal. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to select the clock with appropriate phase in AAPA system, when both discrete clocks and the interpolated clock according to phase select signal lead or lag input data i.e. if the phase difference is such that the incoming data is not falling in the consecutive phase steps. One would have been motivated to



adjust the phase selector in order to switch it to the next or previous phase step depending on if the recovered signal is leading or lagging the input.

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Hendrickson (US 2002/0090045), and Chen (US 5,850,422) further in view of Cranford, JR. et al. (US 2004/0170244).

Claim 10: AAPA, Hendrickson, and Chen disclose a clock and data recovery circuit as in claim 8 above, but neither explicitly discloses that the primary phase selector is comprised of plurality of inverters and at least one interpolated clock can be formed by two consecutive discrete clocks. However, Cranford discloses a similar clock data recovery circuit comprising a sampling phase adjusting unit i.e. a phase selector using inverter to generate a sample phase clock by the interpolator (paragraph 0019; figure 3). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the phase interpolator that uses inverters of different width length (W/L) proportions to generate the interpolated clock from two consecutive discrete clocks in AAPA system. One would have been motivated to implement the above described inverter based interpolator in order to generate variety of interpolated clocks, and to easily correct or adjust the phase of sample interpolated clock if necessary.

***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Sou (US 2003/0161430) discloses a clock and data recovery circuit comprising sampler, selector, phase detector, interpolator etc.

b. Glenn et al. (US 7,197,101) discloses a similar clock and data recovery circuit using a phase interpolator to generate a sample interpolated signal.

c. Saeki (US 7,187,727) discloses a similar clock and data recovery circuit using inverter in phase interpolator to generate a sample interpolated signal.

d. Evans et al. (US 6,002,279) discloses a similar clock and data recovery circuit where the interpolated clock signal is generated between two adjacent phases using an interpolator.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hirdepal Singh whose telephone number is 571-270-1688. The examiner can normally be reached on Mon-Fri (Alternate Friday Off) 8:00AM-5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571-272-3021. The fax phone

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number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HS  
June 14, 2007

Mohammed Ghayour  
SPE 2611

  
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